Contact Resistance of Tri-layer Graphene Side Contacted with Nickel Electrodes

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Abstract

High contact resistance is a key problem in graphene-type device performance. In order to create devices with high performance values such as field effect transistors that operate in the terahertz range, the contact properties of graphene devices requires further research. Nickel's high work-function and contact properties, in conjunction with various layers of graphene, has the potential to lower the contact resistance in field effect transistors. Low contact resistance is difficult to achieve in side-contacted single or multiple-layered graphene devices. The added layers of graphene may improve the contact properties and promises high performance operation in the Terahertz range.

This project was to determine and report the electrical contact properties of nickel to tri-layer graphene, using the side-contacted method and altering the channel length of the graphene. The mechanical exfoliation method was used to obtain Tri-layer graphene samples and then transferred to the SiO_2 covered Si substrates. The graphene was then patterned to the desired widths using the Electron Beam patterning and O_2 plasma etching. The electrodes were then patterned using EB patterning and then the Au-covered Ni electrodes were deposited using EB deposition. Raman spectroscopy and atomic force microscopy (AFM) was employed to determine the number of layers of graphene. The graphene layers were also verified using a separate sample that was characterized, in the same manner, as single, double, tri, and quad layer graphene and then directly compared to the device's tri-layer graphene ribbon. Scanning electron microscopy (SEM) images were taken at the contact points for further visualization of the contact features and the graphene ribbon. The contact resistance and the field-effect modulation were then recorded by using the semiconductor parameter analyzer with the Si substrate as the back-gate. The contact resistance was measured to be 436.5 Ω µm. This low contact resistance plays an important part in the electrical characteristics and is discussed in this work.

Low Contact Resistance between Nickel Electrodes and Side Contacted Tri-layer Graphene Devices

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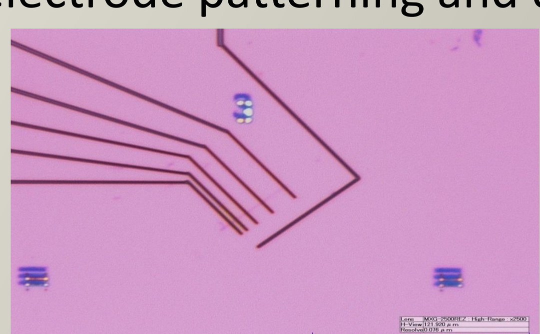
High Speed FET

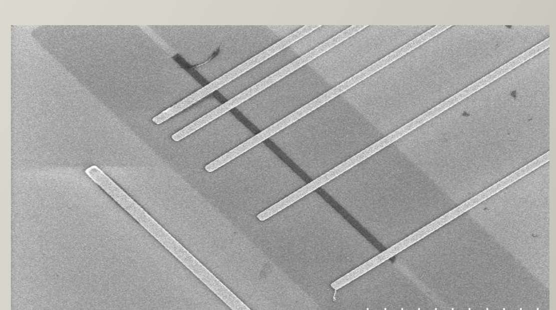
Evaluate the contact resistance properties between Nickel electrodes and tri-layer graphene ribbons for the application of high performance transistors that operate in the terahertz range.

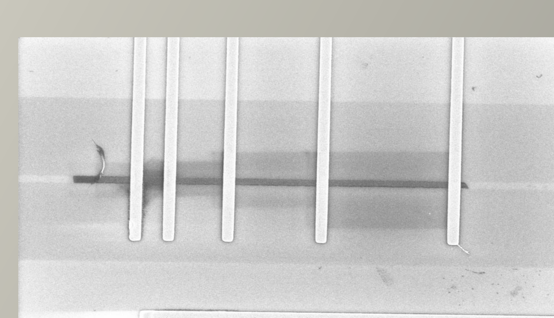
Fabrication

Deposit contacts and patterns to SiO2/Si substrate. Mechanically exfoliate graphite sample and transferred to substrate. Utilized O2 Etching to cut graphene to the desired width of 450 nm and remove excess. Graphene ready for electrode patterning and deposition.

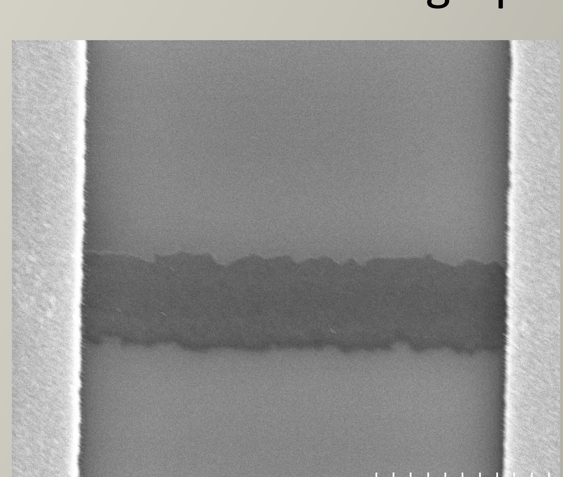


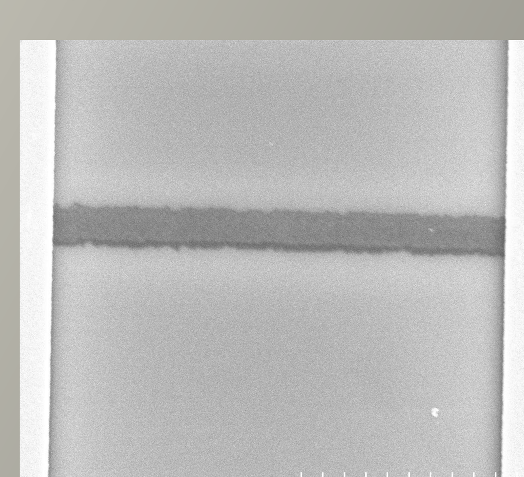
Patterned electrodes are deposited via EB deposition.





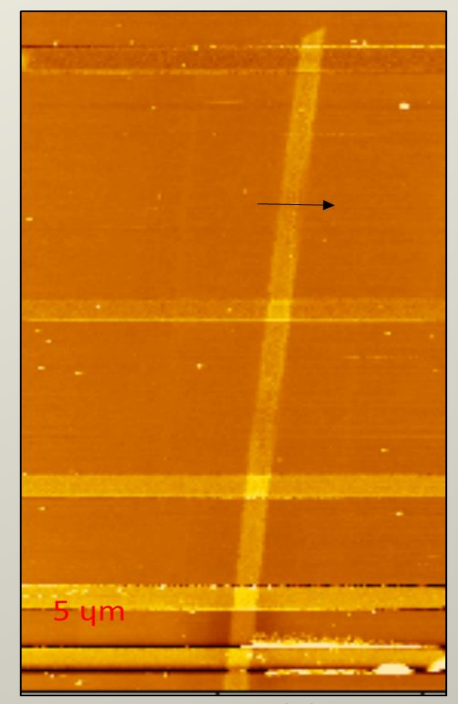
Graphene Channel lengths are increased from 1.1 μm through 4.1 μm in increments of 1 μm on a tri-layer, graphene ribbon.



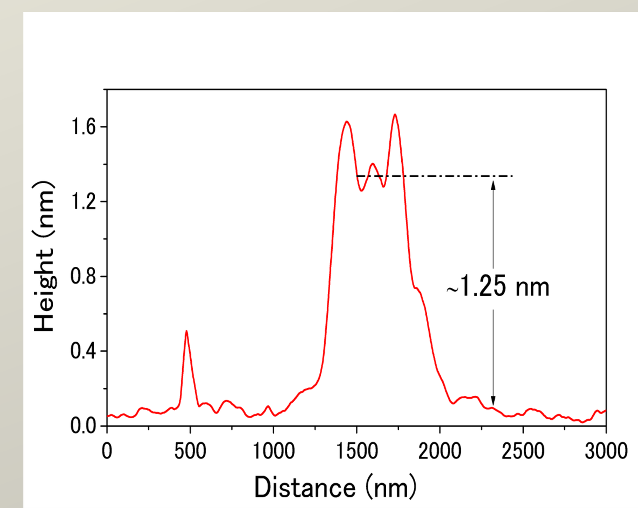


SEM images of the graphene ribbon

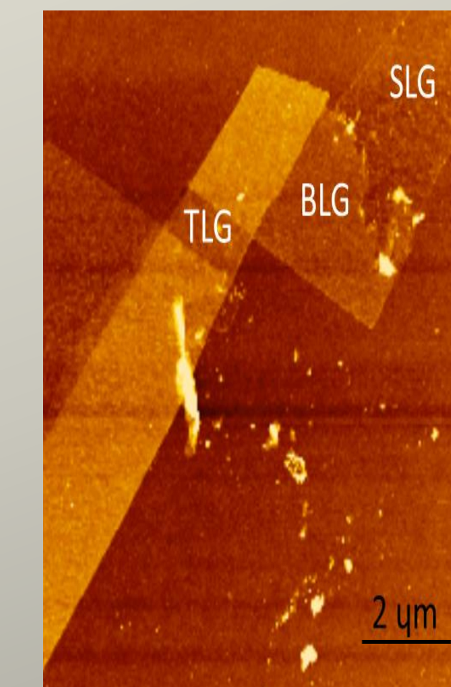
Layer Confirmation Data



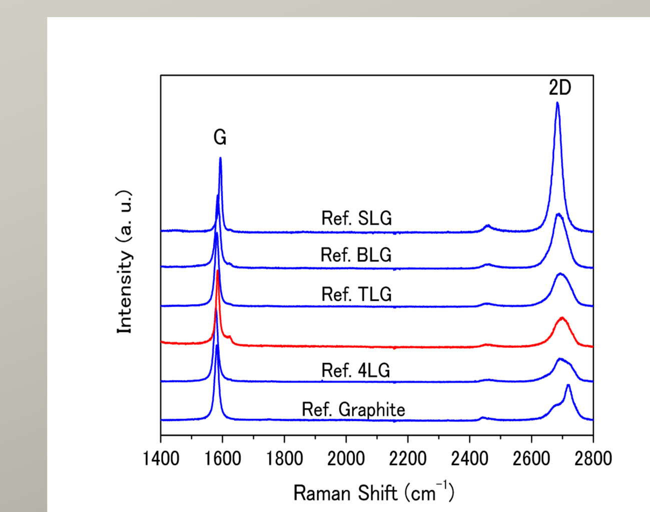
Cross-sectional line profile taken from arrow marked in the AFM image



Height ~ 1.25 nm → Trilayer graphene



AFM image of reference graphene layers



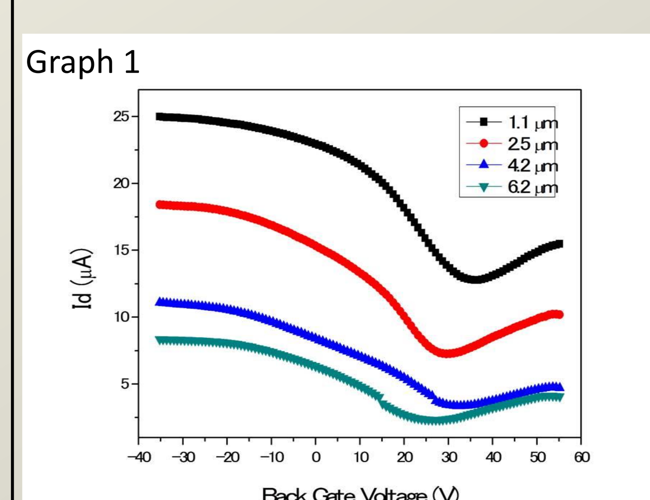
Raman spectra taken from reference graphene layers

Electrical Properties

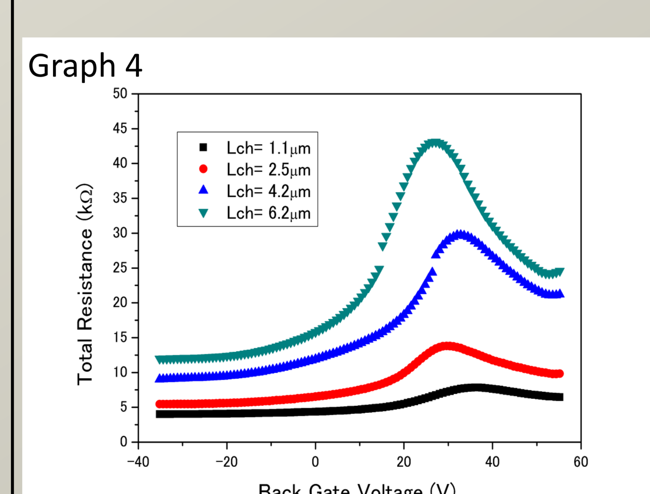
Transfer characteristics of tri-layer graphene device

Pre-annealed

Graph 1

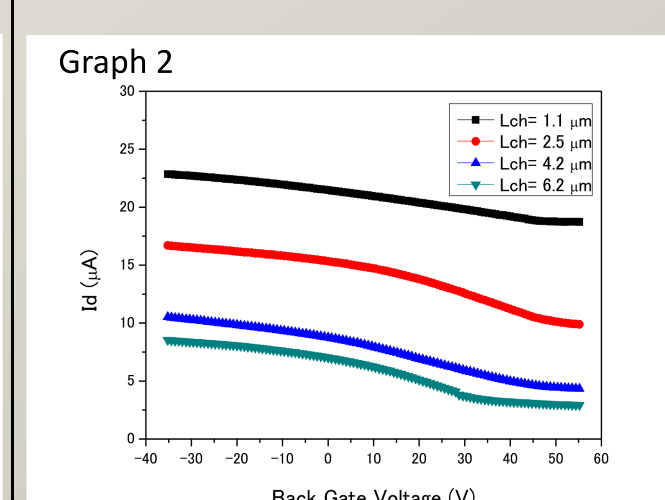


Graph 4

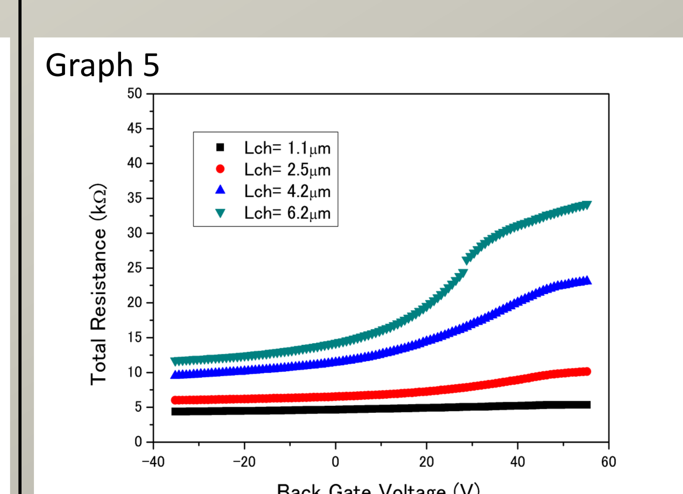


Annealed

Graph 2

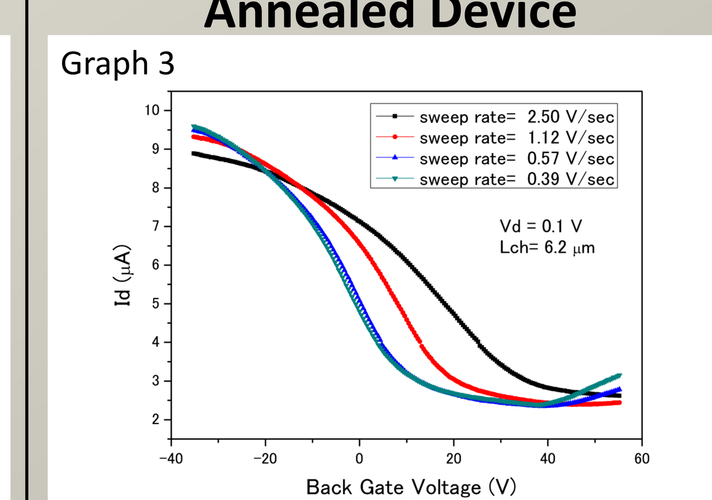


Graph 5



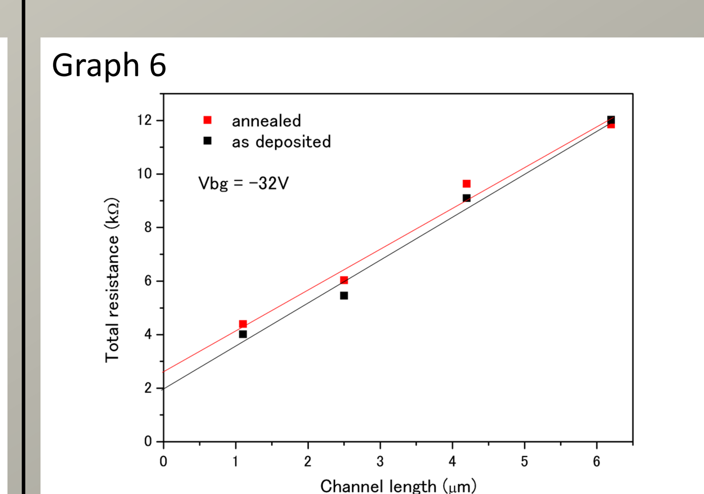
Sweep Rate Characteristics of Annealed Device

Graph 3



Contact Resistance

Graph 6



Contact Resistance

Before annealing
Channel Width: 450 nm
2Rc = 1940 Ω →
Rc = 970 Ω →
Rc = 436.5 Ω.μm

Annealed 200 C at 20 minutes
Channel Width: 450 nm
2Rc = 2650 Ω →
Rc = 1325 Ω →
Rc = 577.7 Ω.μm

Keithley 4200, Semiconductor Parameter Analyzer use for measurements V_d = 100mV V_g = (-35V to 55V)

Summary

We found that tri-layer graphene shows good potential for use as a high-performance field-effect transistor. However we encountered strange phenomenon after annealing the device. The Contact resistance increased and the gate modulation slowed. The reasons for this unexpected behavior are unclear at present. One possibility may be the presence of remnant resist materials on the SiO2 surface, before the graphene was transferred. The presence of the resist might decrease the effective electric field during the application of gate voltage. More research is required, however, to clarify this point. Future plans include adding a top gate and etching away the SiO2 substrate to study this device.

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